Revision History

Rev. No.	History	Issue Date
2.0	Initial issue with new naming rule	Dec. 29, 2004
2.1	Update the WRITE CYCLE1 (Write Enable Controlled) waveform	Mar. 31, 2005
2.2	Revise V_{IL} from 1.5V to 0.8V	Apr. 08, 2005
2.3	Revise V_{IH}, V_{OH}, I_{OL}, I_{CC}, I_{CCSB}, I_{CCSB1}, V_{DR}, I_{CCDR}, t_{DW}	May. 26, 2005
2.4	Add 28L PDIP 300mil	Jul. 04, 2005
2.5	Revise I_{CCSB}, I_{CCSB1} & I_{CCDR}	Oct. 06, 2005
2.6	Revise page 7 data retention waveform (VDR: 1.5V to 2V)	May. 16, 2006
2.7	Revise DC characteristics	Dec. 13, 2006

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■ GENERAL DESCRIPTION

The CS18LV02565 is a high performance, high speed and super low power CMOS Static Random Access Memory organized as 32,768 words by 8bits and operates for a single 4.5 to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed, super low power features and maximum access time of 55/70ns in 5.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE).

The CS18LV02565 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV02565 is available in JEDEC standard 28-pin TSOP I (8x13.4 mm), SOP (330 mil), PDIP (600 mil) and PDIP (300 mil) packages.

■ FEATURES

- Wide operation voltage : 4.5 ~ 5.5V
- Ultra low power consumption : 2mA@1MHz (Max.) , Vcc=5.0V.
  10 uA (Max.) CMOS standby current
- High speed access time : 55/70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 2.0V.
- Easy expansion with /CE and /OE options.

■ PRODUCT FAMILY

Product Family	Operating Temp.	Vcc Range	Speed (ns)	Standby Current(typ.) I_{CCSB1}	Package Type
CS18LV02565	0~70°C	4.5~5.5V	55/70	1.5 uA (Vcc = 5.0V)	28 SOP
					28 TSOP I
					28 PDIP
					Dice
	-40~85°C		55/70	2.0 uA (Vcc= 5.0V)	28 SOP
					28 TSOP I
					28 PDIP
					Dice

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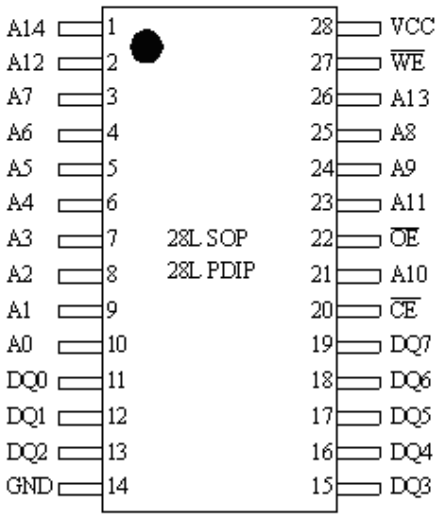
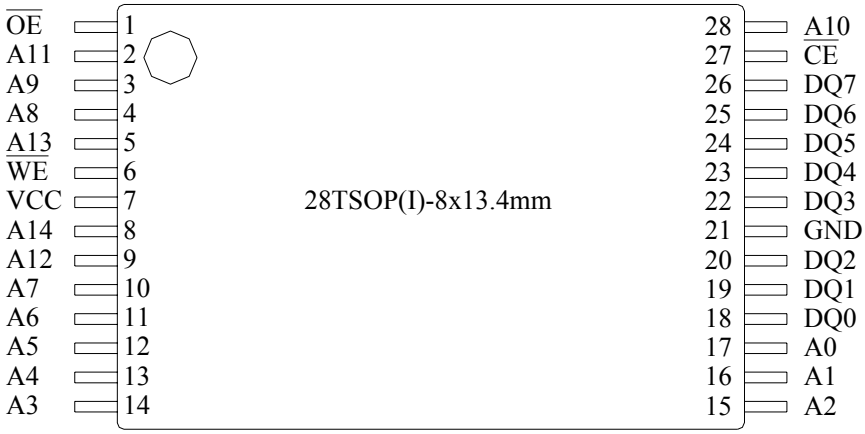
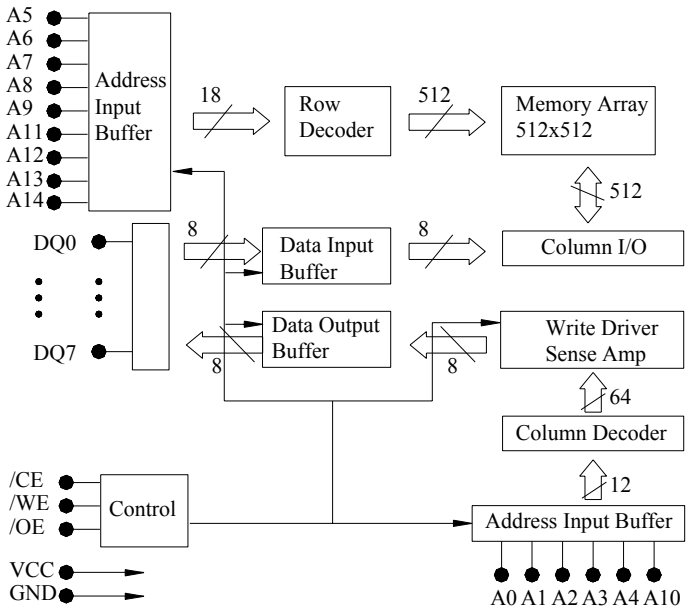
■ PIN CONFIGURATIONS





■ FUNCTIONAL BLOCK DIAGRAM



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■ PIN DESCRIPTIONS

Name	Type	Function
A0 – A14	Input	Address inputs for selecting one of the 32,768 x 8 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
DQ0~DQ7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Gnd	Power	Ground

■ TRUTH TABLE

Mode	/CE	/WE	/OE	DQ0~7	Vcc Current
Standby	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	High Z	I_{CC}
Read	L	H	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

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■ ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage, Vcc	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70°C	4.5~5.5V
Industrial	-40~85°C	4.5~5.5V

■ CAPACITANCE(1)(TA=25℃,f=1.0MHz)

Symbol	Parameter	Conduction	MAX.	Unit
C_{IN}	Input Capacitance	VIN=0V	6	pF
C_{DQ}	Input/Output Capacitance	VI/O=0V	8	pF

1. This parameter is guaranteed, and not 100% tested.

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■ DC ELECTRICAL CHARACTERISTICS (TA = 0° ~70°C, Vcc = 5.0V)

Name	Parameter	Test Condition	MIN	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage	Vcc=5.0V	-0.5(1)	0.8	V
V_{IH}	Guaranteed Input High Voltage	Vcc=5.0V	2.2	Vcc+0.2(2)	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}	-1	1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE=V_{IN}, or /OE=V_{IN}, V_{IO}=0V to V_{CC}	-1	1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1mA	2.4		V
I_{CC}	Operating Power Supply Current	/CE=V_{IL}, I_{DQ}=0mA, F=F_{MAX} =1/ t_{RC}		30	mA
I_{CCSB}	TTL Standby Supply	/CE=V_{IH}, I_{DQ}=0mA,		2.0	mA
I_{CCSB1}	CMOS Standby Current	/CE≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V,		10	uA

1. Undershoot : -2.0V in case of pulse width ≤ 20ns
2. Overshoot : Vcc +2.0V in case of pulse width ≤ 20ns

■ DATA RETENTION CHARACTERISTICS (TA = 0° ~70°C)

Name	Parameter	Test Condition	MIN	T_{yp} (2)	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CE ≧ V_{CC}-0.2V, V_{IN} ≧ V_{CC}-0.2V or V_{IN}≦0.2V	2.0			V
I_{CCDR}	Data Retention Current	/CE≧V_{CC}-0.2V, V_{CC}=2V V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V		0.5	2.0	uA
T_{CDR}	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC} (1)			ns

1. t_{RC}= Read Cycle Time.
2. TA=25°C

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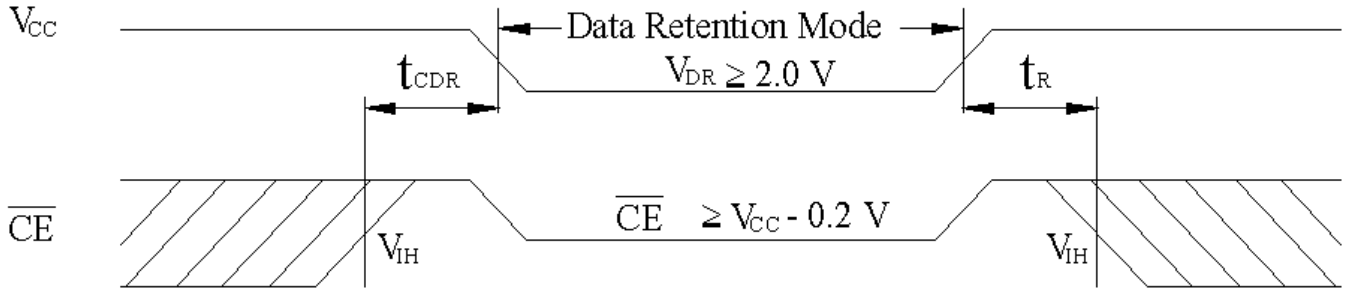
■ LOW Vcc DATA RETENTION WAVEFORM (/CE Controlled)



■ AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc

■ KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

■ AC TEST LOADS AND WAVEFORMS

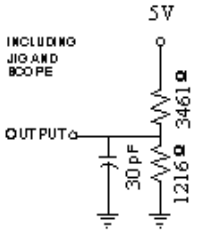


FIGURE 1A

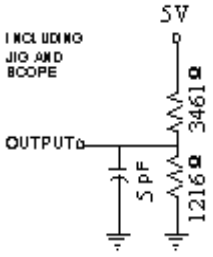


FIGURE 1B

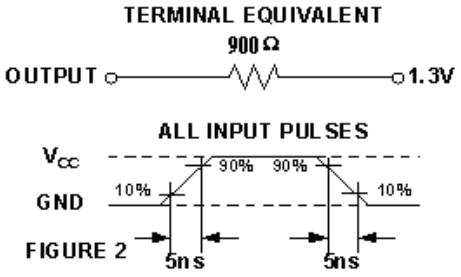


FIGURE 2

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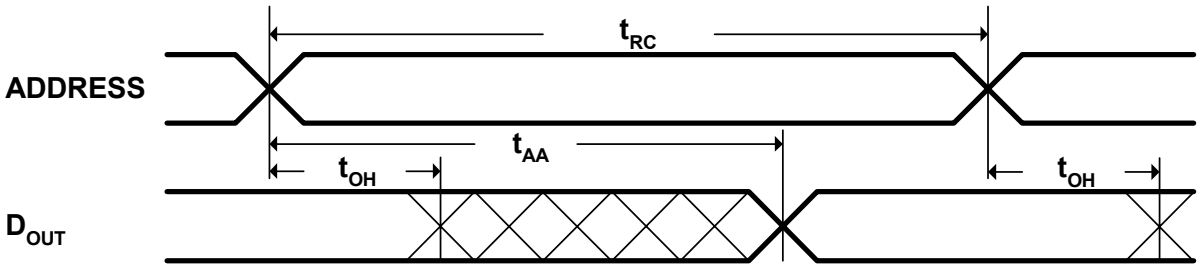
■ AC ELECTRICAL CHARACTERISTICS (TA = 0° ~70°C, Vcc = 5.0V)

< READ CYCLE >

JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{RC}	Read Cycle Time	55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		55		70	ns
t_{ELQV}	t_{ACE}	Chip Select Access Time		55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		30		50	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z	10		10		ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z	0	35	0	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	30	ns
t_{AXOX}	t_{OH}	Address Change to Out Disable	10		10		ns

■ SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE1 (1,2,4)



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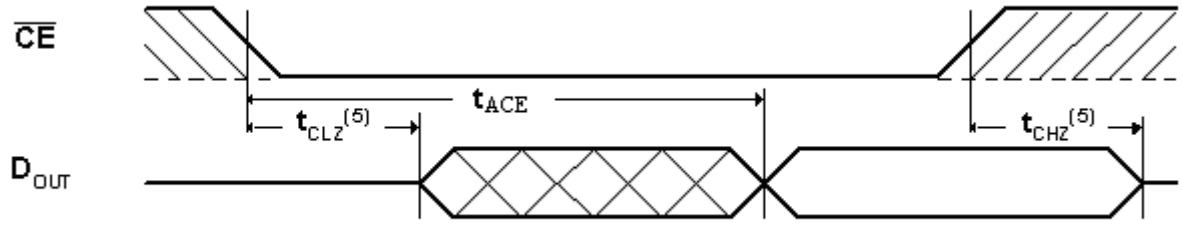
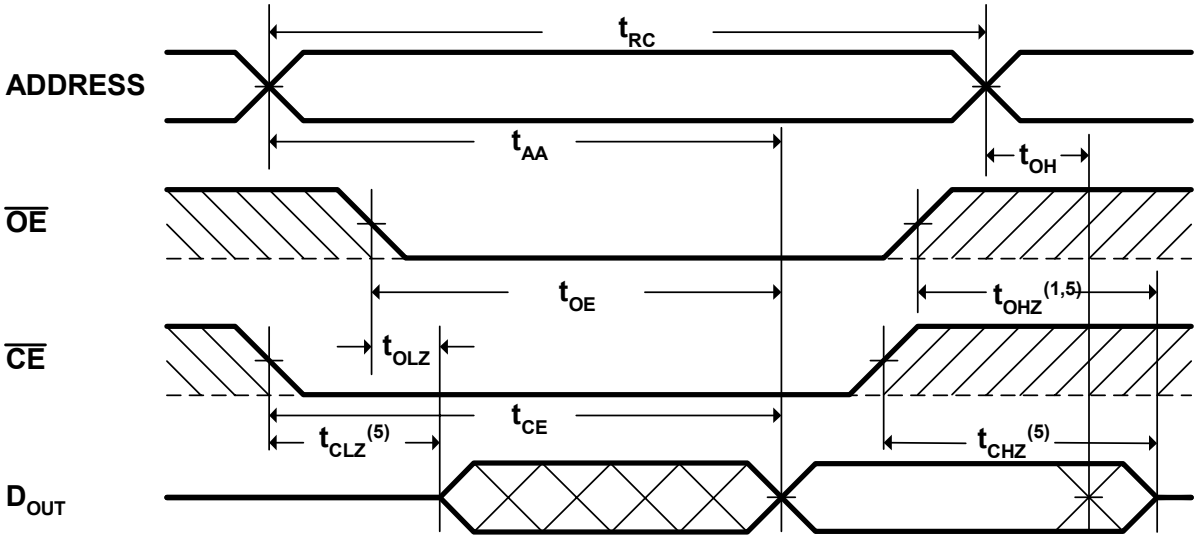
READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:

1. /WE is high in read Cycle.
2. Device is continuously selected when /CE = $V_{IL.}$
3. Address valid prior to or coincident with CE transition low.
4. /OE = VIL.
5. Test conditions assume signal transition times of 5ns or less, timing reference levels of 0.5VCC, input pulse levels of 0V to VCC and output loading specified in Figure 1A.
6. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

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■ AC ELECTRICAL CHARACTERISTICS (TA = 0° ~70°C, Vcc = 5.0V)

< WRITE CYCLE >

JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	55		70		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	55		70		ns
t_{WLWH}	t_{WP}	Write Pulse Width	40		50		ns
t_{WHAX}	t_{WR}	Write Recovery Time	0		0		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		25		35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	20		30		ns
t_{WHDX}	t_{DH}	Data Hold for Write End	0		0		ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	30	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		5		ns

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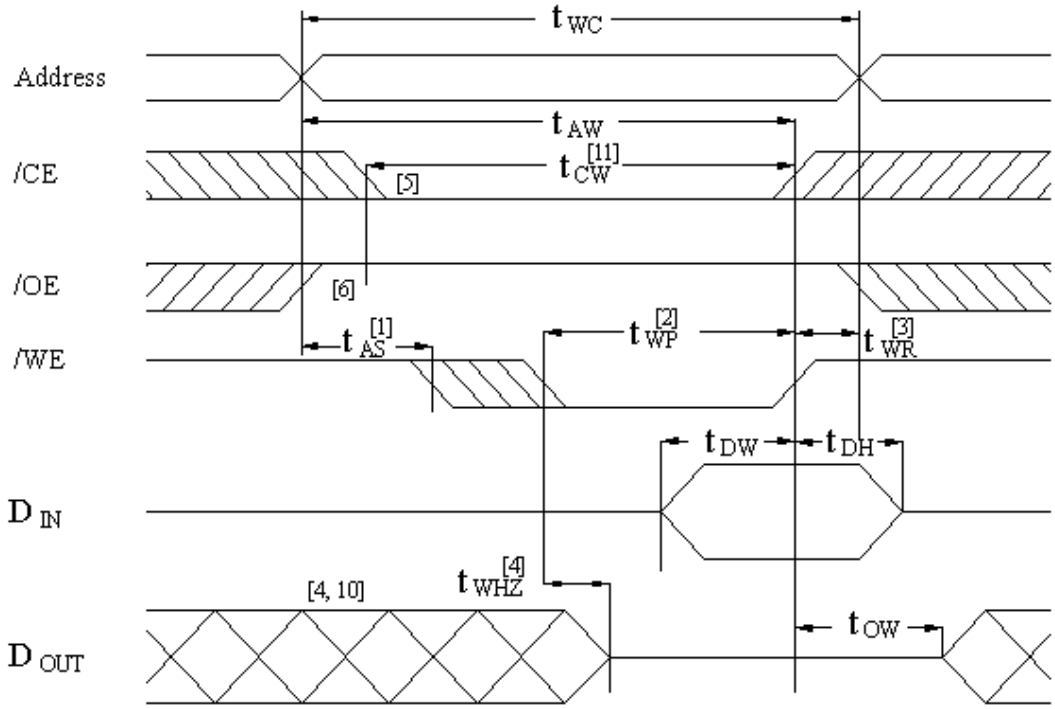
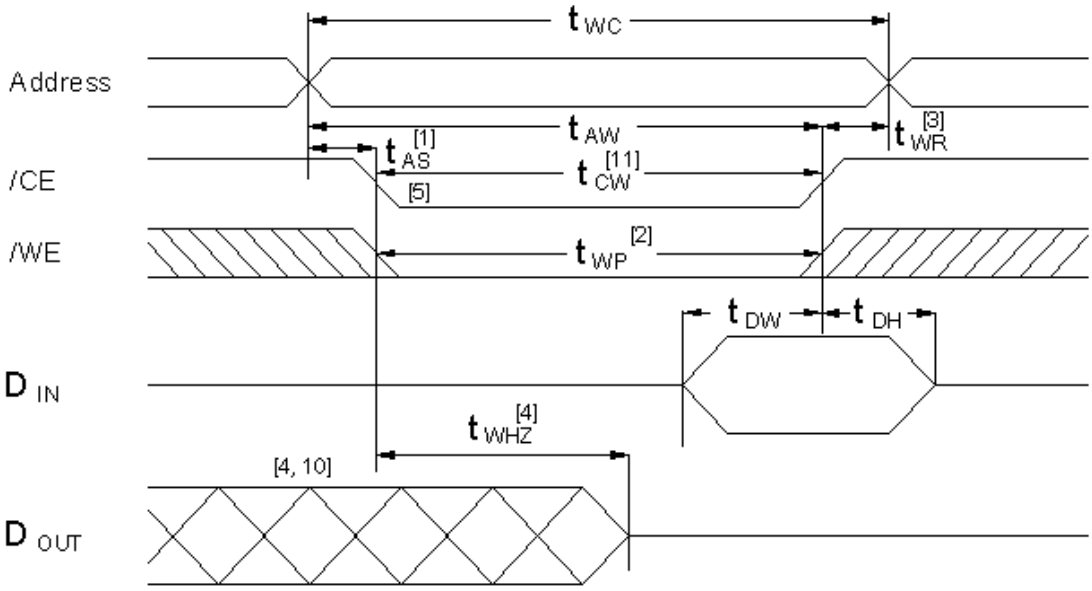
■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (Write Enable Controlled)



WRITE CYCLE2 (Chip Enable Controlled)



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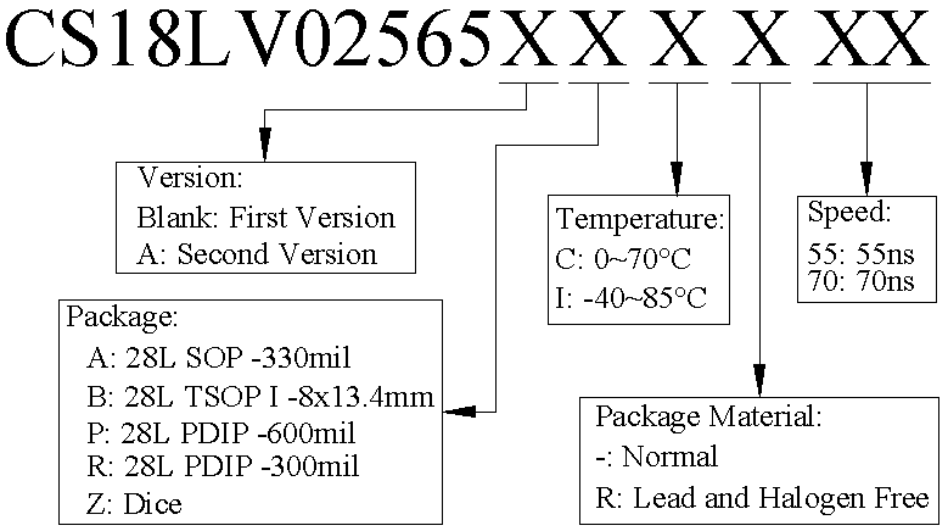
NOTES:

1. /WE must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of /CE and /WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of /CE or /WE going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the /CE low transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.
6. It's recommended to keep /OE at high (/OE = VIH) as /WE Controlled WRITE CYCLE.
7. D_{OUT} is the read data of next address.
8. If /CE is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Test conditions assume signal transition times of 5ns or less, timing reference levels of 0.5VCC, input pulse levels of 0V to VCC and output loading specified in Figure 1A.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of /CE going low to the end of write.

■ ORDER INFORMATION



Note: Package material code "R" meets ROHS

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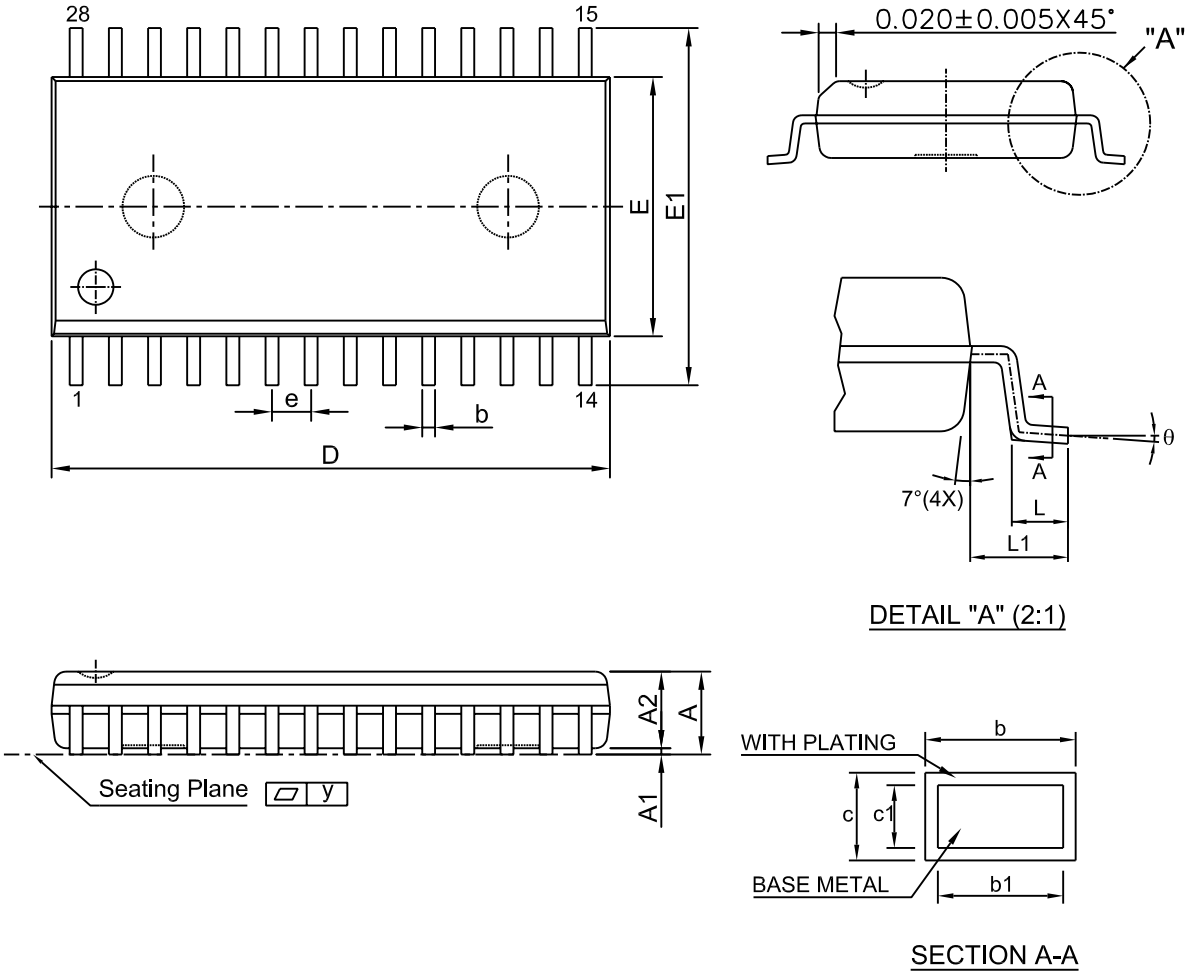
■ PACKAGE DIMENSIONS - 28L SOP -330mil



SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	Θ
mm	Min.	2.540	0.102	2.362	0.35	0.35	0.20	0.20	17.983	8.280	11.506	1.118	0.700	1.520	–	0°
	Nom.	2.692	0.226	2.489	–	–	–	–	18.110	8.407	11.811	1.270	0.964	1.720	–	–
	Max.	2.844	0.350	2.616	0.50	0.45	0.32	0.28	18.237	8.534	12.116	1.422	1.228	1.920	0.1	10°
inch	Min.	0.100	0.004	0.093	0.014	0.014	0.008	0.008	0.708	0.326	0.453	0.044	0.0276	0.0598	–	0°
	Nom.	0.106	0.009	0.098	–	–	–	–	0.713	0.331	0.465	0.050	0.0380	0.0677	–	–
	Max.	0.112	0.014	0.103	0.020	0.018	0.012	0.011	0.718	0.336	0.477	0.056	0.0484	0.0756	0.004	10°

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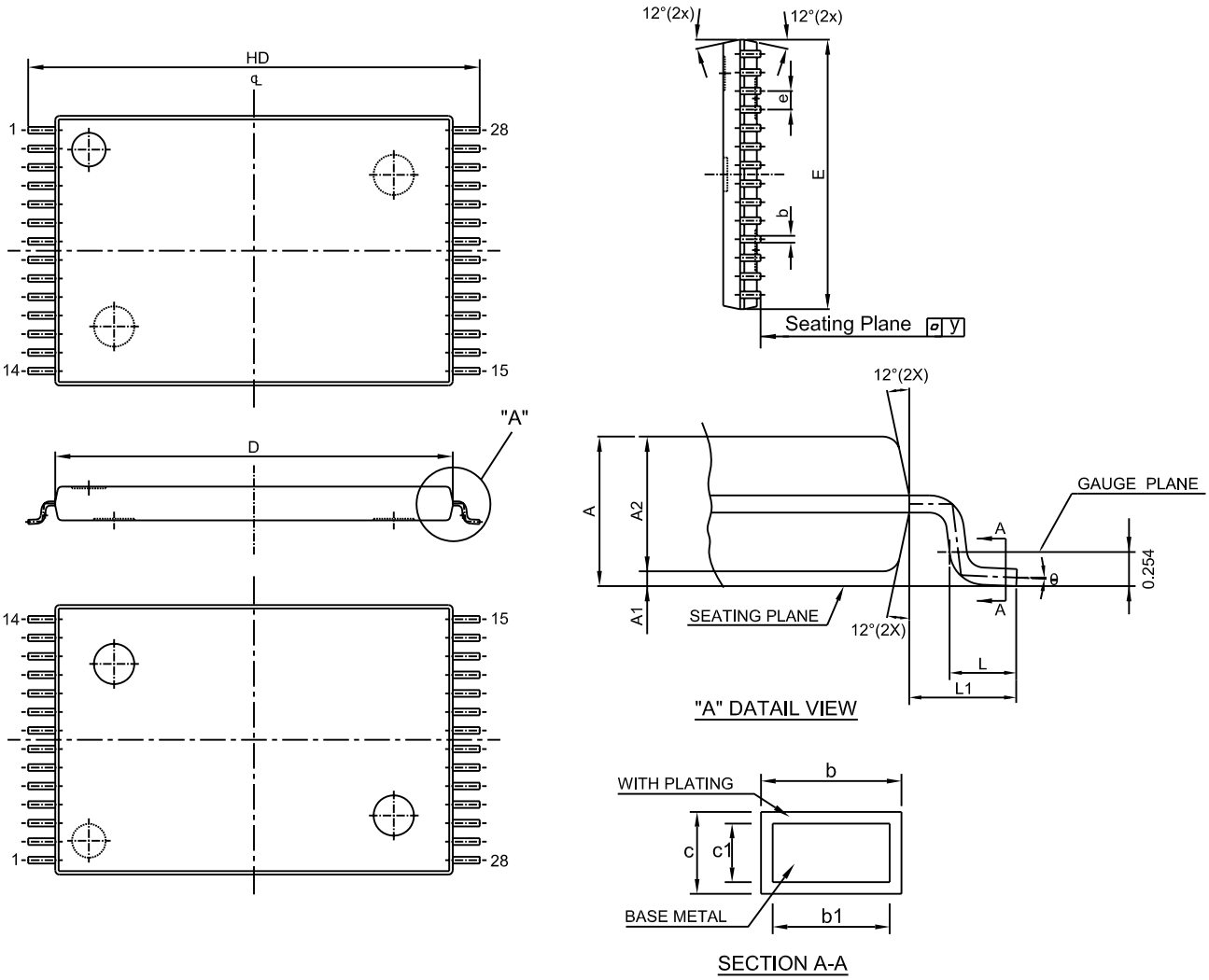
■ PACKAGE DIMENSIONS - 28L TSOP 1- 8x13.4mm



SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	Θ
mm	Min.	1.00	0.050	0.95	0.17	0.17	0.10	0.10	11.70	7.90	0.45	13.20	0.40	0.70	–	0°
	Nom.	1.10	0.115	1.00	0.22	0.20	–	–	11.80	8.00	0.55	13.40	0.50	0.80	–	–
	Max.	1.20	0.180	1.05	0.27	0.23	0.21	0.16	11.90	8.10	0.65	13.60	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.0019	0.037	0.007	0.007	0.004	0.004	0.461	0.311	0.018	0.520	0.0157	0.0275	–	0°
	Nom.	0.0433	0.0045	0.039	0.009	0.008	–	–	0.465	0.315	0.022	0.528	0.0197	0.0315	–	–
	Max.	0.0473	0.0071	0.041	0.011	0.009	0.008	0.006	0.469	0.319	0.026	0.536	0.0277	0.0355	0.004	8°

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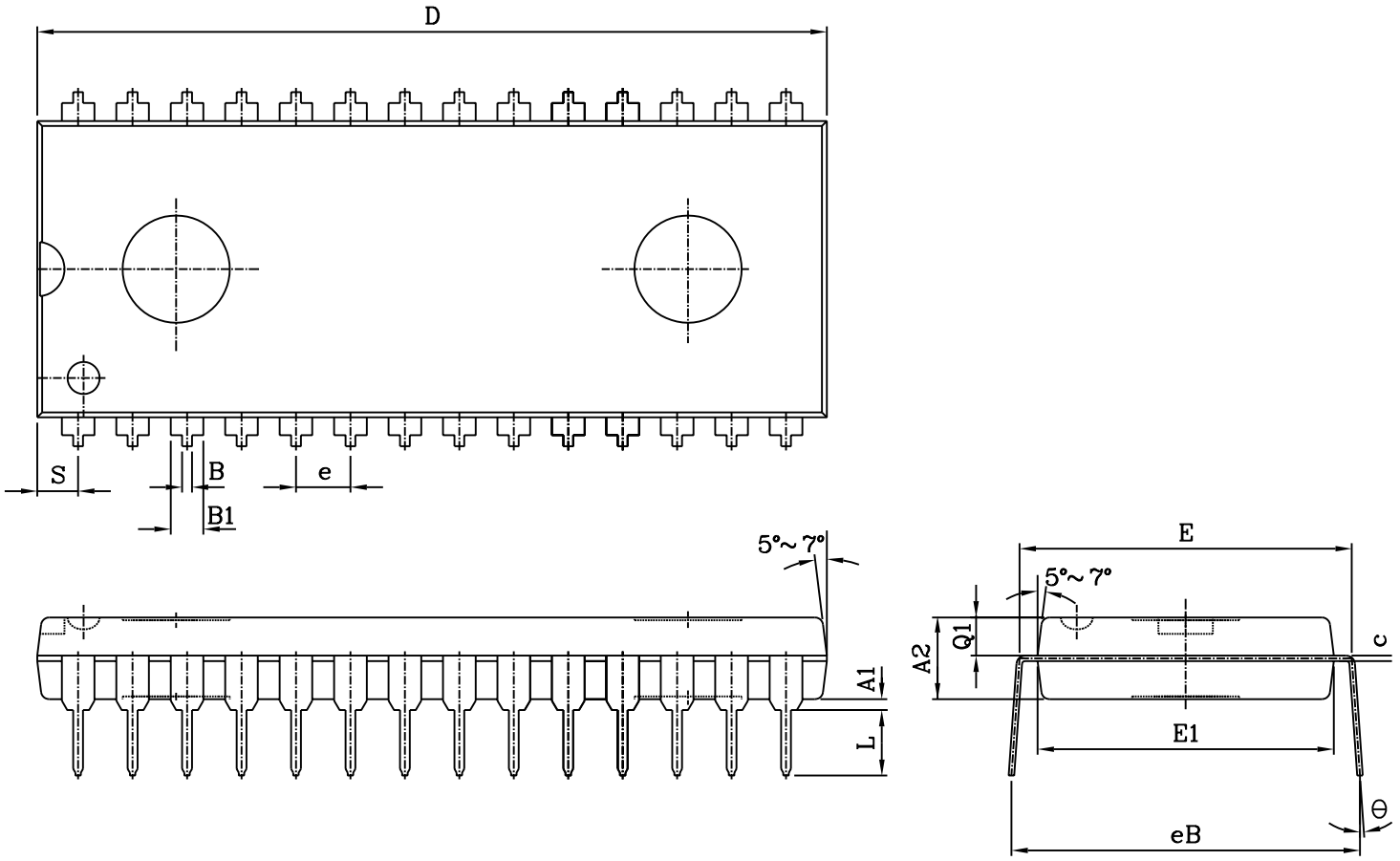
■ PACKAGE DIMENSIONS - 28L PDIP -600mil



SYMBOL / UNIT		A1	A2	B	B1	c	D	E	E1	e	eB	L	S	Q1	Θ
mm	Min.	0.254	3.683	0.330	1.270	0.152	36.957	14.986	13.716	2.540 (TYP)	15.748	3.048	1.778	1.651	3°
	Nom.	–	3.810	0.457	1.524	0.254	37.084	15.240	13.818		16.256	3.302	2.032	1.778	6°
	Max.	–	3.937	0.584	1.778	0.356	37.211	15.494	13.920		16.764	3.556	2.286	1.905	9°
inch	Min.	0.010	0.145	0.013	0.050	0.006	1.455	0.590	0.540	0.100 (TYP)	0.620	0.120	0.070	0.065	3°
	Nom.	–	0.150	0.018	0.060	0.010	1.460	0.600	0.544		0.640	0.130	0.080	0.070	6°
	Max.	–	0.155	0.023	0.070	0.014	1.465	0.610	0.548		0.660	0.140	0.090	0.075	9°

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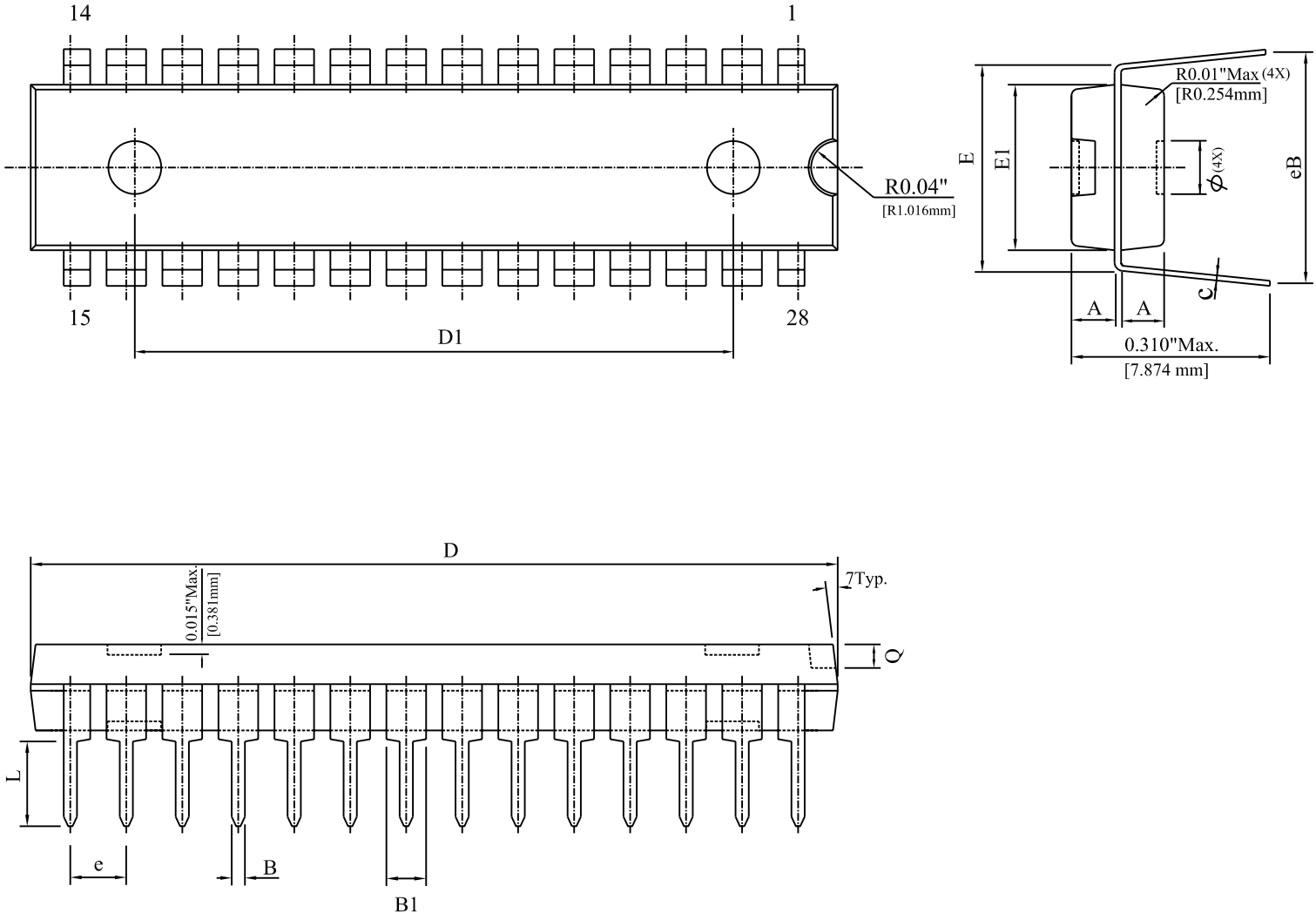
Title: Package outline for 28L PDIP-300mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	B	B1	c	D	D1	E	E1	e	eB	L	Q	ϕ
mm	Min.	1.422	0.406	1.397	-	35.001	27.305	7.366	7.264	2.540 (TYP)	8.382	2.921	0.762	1.778
	Nom.	1.524	0.457	1.524	0.254	35.255	27.559	7.874	7.366		8.890	-	0.889	2.032
	Max.	1.626	0.508	1.651	-	35.509	27.813	8.382	7.468		9.398	-	1.016	2.286
inch	Min.	0.056	0.016	0.055	-	1.378	1.075	0.290	0.286	0.100 (TYP)	0.330	0.115	0.030	0.070
	Nom.	0.060	0.018	0.060	0.01	1.388	1.085	0.310	0.290		0.350	-	0.035	0.080
	Max.	0.064	0.020	0.065	-	1.398	1.095	0.330	0.294		0.370	-	0.040	0.090

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